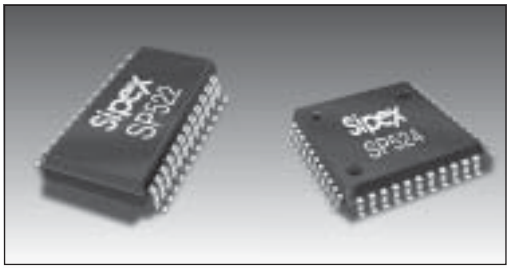
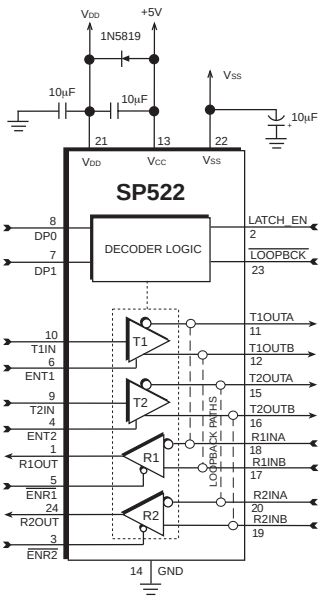
# Low-Cost Programmable Multi-Protocol Transceivers

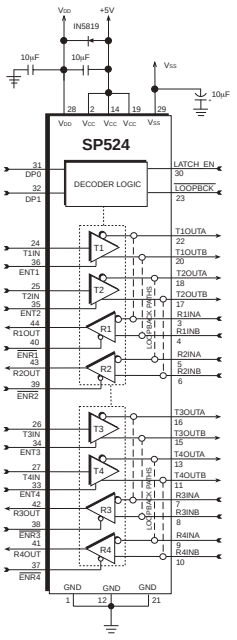
- SP522 — 2 Drivers and 2 Receivers
- SP524 — 4 Drivers and 4 Receivers
- Driver and Receiver Tri-State Control
- Low-Cost WAN Solution
- Loopback Function for Diagnostics
- Software Selectable Interface Modes:
  - -RS-232 (V.28), RS-423 (V.10)
  - -RS-422 (V.11, X.21), RS-485




## DESCRIPTION

The **SP522/524** is a monolithic device that supports three serial interface standards for Wide Area Network Connectivity. The **SP522/524** is ideally suited for multi-protocol designs that are cost and space sensitive. The **SP522/524** is fabricated using a low power BiCMOS process technology. Two (2) drivers and two (2) receivers for the **SP522** can be configured via software for any of the above interface modes at any time. The **SP524** offers two (2) additional drivers and two (2) additional receivers.



## SPECIFICATIONS

Typical @ 25°C and nominal supply voltages unless otherwise noted.

| | MIN. | TYP. | MAX. | UNITS | CONDITIONS |
|---|---|---|---|---|---|
| **LOGIC INPUTS** | | | | | |
| $V_{IL}$ | | | 0.8 | Volts | |
| $V_{IH}$ | 2.0 | | | Volts | |
| **LOGIC OUTPUTS** | | | | | |
| $V_{OL}$ | | | 0.4 | Volts | $I_{OUT}$ = –3.2mA |
| $V_{OH}$ | 2.4 | | | Volts | $I_{OUT}$ = 1.0mA |
| **RS422 DRIVER** | | | | | |
| TTL Input Levels | | | | | |
| $V_{IL}$ | 0 | | 0.8 | Volts | |
| $V_{IH}$ | 2.0 | | | Volts | |
| Outputs | | | | | |
| Differential Output | ±2.0 | | ±5.0 | Volts | R=50Ω; see Figure 1 |
| Open Circuit Voltage,$V_O$ | | | ±6.0 | Volts | |
| Balance | | | ±0.4 | Volts | $\lvert V_T\rvert - \lvert\overline{V_T}\rvert$ |
| Offset | | | +3.0 | Volts | |
| Short Circuit Current | | | ±150 | mA | $V_{out}$ = 0V |
| Power Off Current | | | ±100 | µA | $V_{cc}$ = 0V, $V_{out}$ = ±0.25V |
| Transition Time | | | 40 | nS | Rise/fall time, 10%-90% |
| Max. Transmission Rate | 10 | | | Mbps | $R_L$=100Ω |
| Propagation Delay | | | | | $T_A$ = +25°C |
| $t_{PHL}$ | | 90 | 150 | nS | $R_{DIFF}$=100Ω, Figures 3 & 5 |
| $t_{PLH}$ | | 90 | 150 | nS | $R_{DIFF}$=100Ω, Figures 3 & 5 |
| **RS422 RECEIVER** | | | | | |
| TTL Output Levels | | | | | |
| $V_{OL}$ | | | 0.4 | Volts | |
| $V_{OH}$ | 2.4 | | | Volts | |
| Input | | | | | |
| High Threshold | +0.3 | | +6.0 | Volts | (a)-(b) |
| Low Threshold | -6.0 | | -0.3 | Volts | (a)-(b) |
| Common Mode Range | -7.0 | | +7.0 | Volts | |
| High Input Current | | | | | Refer to Rec. input graph |
| Low Input Current | | | | | Refer to Rec. input graph |
| Receiver Sensitivity | | | ±0.3 | Volts | $V_{CM}$ = +7V to -7V |
| Input Impedance | 4 | | | kΩ | |
| Max. Transmission Rate | 10 | | | Mbps | |
| Propagation Delay | | | | | $T_A$ = +25°C |
| $t_{PHL}$ | | 110 | 175 | nS | Figures 3 & 7 |
| $t_{PLH}$ | | 110 | 175 | nS | Figures 3 & 7 |
| **RS485 DRIVER** | | | | | |
| TTL Input Levels | | | | | |
| $V_{IL}$ | | | 0.8 | Volts | |
| $V_{IH}$ | 2.0 | | | Volts | |
| Outputs | | | | | |
| Differential Output | ±1.5 | | ±5.0 | Volts | R=27Ω; $C_L$=50pF; see Fig. 1 |
| Open Circuit Voltage,$V_O$ | | | ±6.0 | Volts | |
| Balance | | | ±0.2 | Volts | $\lvert V_T\rvert - \lvert\overline{V_T}\rvert$ |
| Output Current | 28.0 | | | mA | $R_L$=54Ω |
| Short Circuit Current | | ±200 | | mA | $V_{out}$ = –7V to +7V |
| Transition Time | | | 40 | nS | Rise/fall time, 10%-90% |
| Max. Transmission Rate | 10 | | | Mbps | $R_L$=54Ω |
| Propagation Delay | | | | | Figures 3 & 5; $T_A$ = +25°C |
| $t_{PHL}$ | | 100 | 150 | nS | $R_{DIFF}$=54Ω, $C_{RL}$ = 50pF |
| $t_{PLH}$ | | 100 | 150 | nS | $R_{DIFF}$=54Ω, $C_{RL}$ = 50pF |

## SPECIFICATIONS

Typical @ 25°C and nominal supply voltages unless otherwise noted.

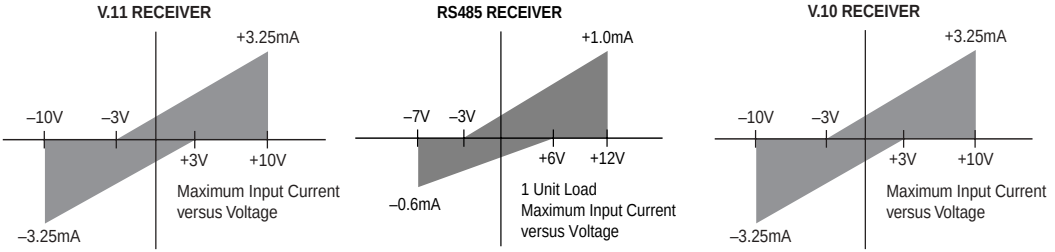
| | MIN. | TYP. | MAX. | UNITS | CONDITIONS |
|---|---|---|---|---|---|
| **RS485 RECEIVER** | | | | | |
| TTL Output Levels | | | | | |
| $V_{OL}$ | | | 0.4 | Volts | |
| $V_{OH}$ | 2.4 | | | Volts | |
| Input | | | | | |
| Common Mode Range | -7.0 | | +12.0 | Volts | |
| High Input Current | | | | | Refer to Rec. input graph |
| Low Input Current | | | | | Refer to Rec. input graph |
| Receiver Sensitivity | | ±0.1 | | Volts | $V_{CM}$ = +12V to -7V |
| Input Impedance | 12 | | | kΩ | $V_{CM}$ = +12V to -7V |
| Max. Transmission Rate | 10 | | | Mbps | |
| Propagation Delay | | | | | $T_A$ = +25°C |
| $t_{PHL}$ | | 110 | 175 | nS | Figures 3 & 7 |
| $t_{PLH}$ | | 110 | 175 | nS | Figures 3 & 7 |
| **RS232 DRIVER** | | | | | |
| TTL Input Level | | | | | |
| $V_{IL}$ | | | 0.8 | Volts | |
| $V_{IH}$ | 2.0 | | | Volts | |
| Outputs | | | | | |
| High Level Output | +5.0 | | +15 | Volts | $R_L$=3KΩ, $V_{IN}$=0.8V |
| Low Level Output | -15.0 | | -5.0 | Volts | $R_L$=3KΩ, $V_{IN}$=2.0V |
| Open Circuit Voltage | -15 | | +15 | Volts | |
| Short Circuit Current | | | ±100 | mA | $V_{out}$ = 0V |
| Power Off Impedance | 300 | | | Ω | $V_{cc}$ = 0V, $V_{out}$ = ±2.0V |
| Slew Rate | | | 30 | V/μs | $R_L$=3KΩ, $C_L$=50pF, between +3V to –3V |
| Transition Time | | | 1.5 | μs | $R_L$=3KΩ, $C_L$=2500pF |
| Max. Transmission Rate | 120 | | | Kbps | $R_L$=3KΩ, $C_L$=2500pF |
| Propagation Delay | | | | | $T_A$ = +25°C |
| $t_{PHL}$ | | 2 | 8 | μS | $R_L$=3KΩ |
| $t_{PLH}$ | | 2 | 8 | μS | $R_L$=3KΩ |
| **RS232 RECEIVER** | | | | | |
| TTL Output Levels | | | | | |
| $V_{OL}$ | | | 0.4 | Volts | |
| $V_{OH}$ | 2.4 | | | Volts | |
| Input | | | | | |
| High Threshold | | 1.7 | 3.0 | Volts | |
| Low Threshold | 0.8 | 1.2 | | Volts | |
| Receiver Open Circuit Bias | | | +2.0 | Volts | |
| Input Impedance | 3 | 5 | 7 | KΩ | |
| Max. Transmission Rate | 120 | | | Kbps | |
| Propagation Delay | | | | | $T_A$ = +25°C |
| $t_{PHL}$ | | 0.2 | 1 | μS | |
| $t_{PLH}$ | | 0.2 | 1 | μS | |
| **RS423 DRIVER** | | | | | |
| TTL Input Levels | | | | | |
| $V_{IL}$ | | | 0.8 | Volts | |
| $V_{IH}$ | 2.0 | | | Volts | |
| Output | | | | | $V_{DD}$ = +5V, $V_{SS}$ = –5V |
| High Level Output | +3.6 | | +6.0 | Volts | $R_L$=450Ω, $V_T$ = 0.9*$V_{OC}$ |
| Low Level Output | -6.0 | | -3.6 | Volts | $R_L$=450Ω, $V_T$ = 0.9*$V_{OC}$ |
| Open Circuit Voltage | ±4.0 | | ±6.0 | Volts | |
| Short Circuit Current | | | ±150 | mA | $V_{OUT}$ = 0V |

## SPECIFICATIONS (Continued)

Typical @ 25°C and nominal supply voltages unless otherwise noted.

| | MIN. | TYP. | MAX. | UNITS | CONDITIONS |
|---|---|---|---|---|---|
| **RS-423 DRIVER** | | | | | |
| Power Off Current | | | ±100 | µA | $V_{CC}$ = 0V, $V_{OUT}$= ±0.25V |
| Transition Time | | | 1.0 | µs | Rise/fall time, 10-90% |
| Max. Transmission Rate | 120 | | | Kbps | $R_L$=450Ω |
| Propagation Delay | | | | | $T_A$ = +25°C |
| $t_{PHL}$ | | 2 | 8 | µS | $R_L$=450Ω |
| $t_{PLH}$ | | 2 | 8 | µS | $R_L$=450Ω |
| **RS423 RECEIVER** | | | | | |
| TTL Output Levels | | | | | |
| $V_{OL}$ | 0 | | 0.4 | Volts | |
| $V_{OH}$ | 2.4 | | | Volts | |
| Input | | | | | |
| High Threshold | +0.3 | | +7.0 | Volts | |
| Low Threshold | -7.0 | | -0.3 | Volts | |
| Common Mode Range | -7.0 | | +7.0 | Volts | |
| High Input Current | | | | | Refer to Rec. input graph |
| Low Input Current | | | | | Refer to Rec. input graph |
| Receiver Sensitivity | | | ±0.3 | Volts | $V_{CM}$ = +7V to -7V |
| Input Impedance | 4 | | | KΩ | $V_{IN}$ = +10V to -10V |
| Max. Transmission Rate | 120 | | | Kbps | |
| Propagation Delay | | | | | $T_A$ = +25°C |
| $t_{PHL}$ | | 0.5 | 1 | µS | |
| $t_{PLH}$ | | 0.5 | 1 | µS | |
| **POWER REQUIREMENTS** | | | | | |
| $V_{CC}$ | +4.75 | +5.0 | +5.25 | Volts | |
| $V_{DD}$ | +9.5 | +10.0 | +10.5 | Volts | |
| $V_{SS}$ | -9.5 | -10.0 | -10.5 | Volts | |
| $I_{CC}$ | | 4 | | mA | $V_{CC}$ = +5V; DP0=DP1=0V |
| $I_{DD}$ | | 10 | | mA | $V_{DD}$ = +10V; DP0=DP1=0V |
| $I_{SS}$ | | 10 | | mA | $V_{SS}$ = –10V; DP0=DP1=0V |
| **ENVIRONMENTAL AND MECHANICAL** | | | | | |
| Operating Temperature Range | 0 | | +70 | °C | |
| Storage Temperature Range | -65 | | +150 | °C | |
| Package | 24-pin SOIC, 24-pin SSOP, 44–pin QFP | | | | |

## RECEIVER INPUT GRAPHS



## ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

$V_{CC}$.....+7V
$V_{DD}$.....+12V
$V_{SS}$.....–12V
Input Voltages
Logic.....-0.5V to ($V_{CC}$+0.5V)
Drivers.....-0.5V to ($V_{CC}$+0.5V)
Receivers.....±30V@≤100mA
Outputs Voltages
Logic.....-0.5V to ($V_{CC}$+0.5V)
Drivers.....±15V
Receivers.....-0.5V to ($V_{CC}$+0.5V)
Storage Temperature.....-65˚C to +150˚C
Power Dissipation.....2000mW

**CAUTION**:
ESD (ElectroStatic Discharge) sensitive device. Permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. Personnel should be properly grounded prior to handling this device. The protective foam should be discharged to the destination socket before devices are removed.

## OTHER AC CHARACTERISTICS

(Typical @ 25°C and nominal supply voltages unless otherwise noted)

| PARAMETER | MIN. | TYP. | MAX. | UNITS | CONDITIONS |
|---|---|---|---|---|---|
| **DRIVER DELAY TIME FROM ENABLE MODE TO TRI–STATE MODE** | | | | | |
| **SINGLE–ENDED MODE (RS-232, RS-423)** | | | | | |
| $t_{PZL}$; Enable to Output low | | 600 | | ns | 3KΩ pull–up to output |
| $t_{PZH}$; Enable to Output high | | 300 | | ns | 3KΩ pull–down to output |
| $t_{PLZ}$; Disable from Output low | | 300 | | ns | 5V to input |
| $t_{PHZ}$; Disable from Output high | | 900 | | ns | GND to input |
| **DIFFERENTIAL MODE (RS-422, RS-485)** | | | | | |
| $t_{PZL}$; Enable to Output low | | 100 | | ns | $C_L$ = 100pF, Fig. 4 & 6; $S_1$ closed |
| $t_{PZH}$; Enable to Output high | | 120 | | ns | $C_L$ = 100pF, Fig. 4 & 6; $S_2$ closed |
| $t_{PLZ}$; Disable from Output low | | 100 | | ns | $C_L$ = 15pF, Fig. 4 & 6; $S_1$ closed |
| $t_{PHZ}$; Disable from Output high | | 160 | | ns | $C_L$ = 15pF, Fig. 4 & 6; $S_2$ closed |
| **RECEIVER DELAY TIME FROM ENABLE MODE TO TRI–STATE MODE** | | | | | |
| **SINGLE–ENDED MODE (RS-232, RS-423)** | | | | | |
| $t_{PZL}$; Enable to Output low | | 125 | | ns | 3KΩ pull–up to output |
| $t_{PZH}$; Enable to Output high | | 120 | | ns | 3KΩ pull–down to output |
| $t_{PLZ}$; Disable from Output low | | 90 | | ns | 5V to input |
| $t_{PHZ}$; Disable from Output high | | 90 | | ns | GND to input |
| **DIFFERENTIAL MODE (RS-422, RS-485)** | | | | | |
| $t_{PZL}$; Enable to Output low | | 125 | | ns | $C_{RL}$ = 15pF, Fig. 2 & 8; $S_1$ closed |
| $t_{PZH}$; Enable to Output high | | 120 | | ns | $C_{RL}$ = 15pF, Fig. 2 & 8; $S_2$ closed |
| $t_{PLZ}$; Disable from Output low | | 90 | | ns | $C_{RL}$ = 15pF, Fig. 2 & 8; $S_1$ closed |
| $t_{PHZ}$; Disable from Output high | | 90 | | ns | $C_{RL}$ = 15pF, Fig. 2 & 8; $S_2$ closed |

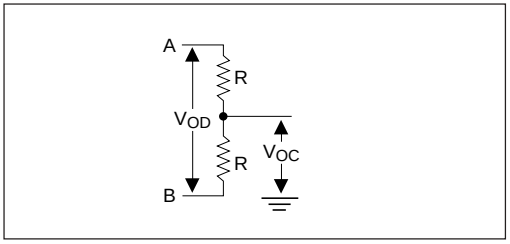



*Figure 1. Driver DC Test Load Circuit*

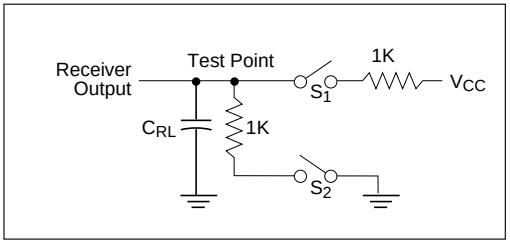



*Figure 2. Receiver Timing Test Load Circuit*

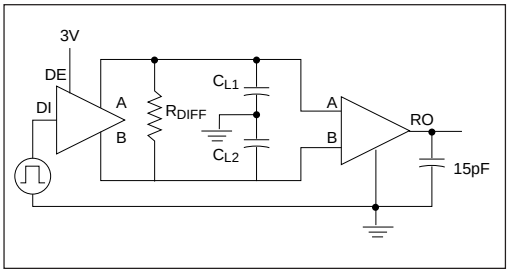



*Figure 3. Driver/Receiver Timing Test Circuit*

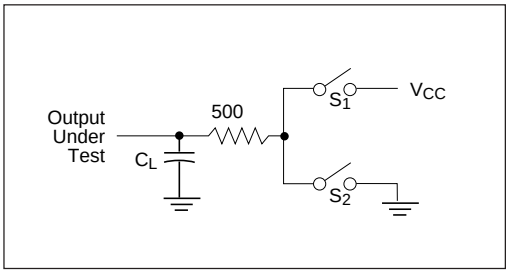



*Figure 4. Driver Timing Test Load #2 Circuit*

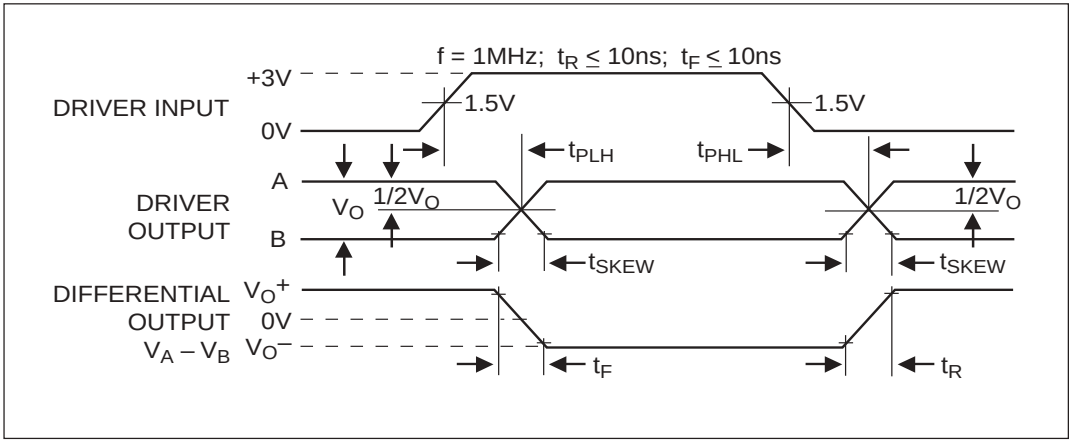



*Figure 5. Driver Propagation Delays*

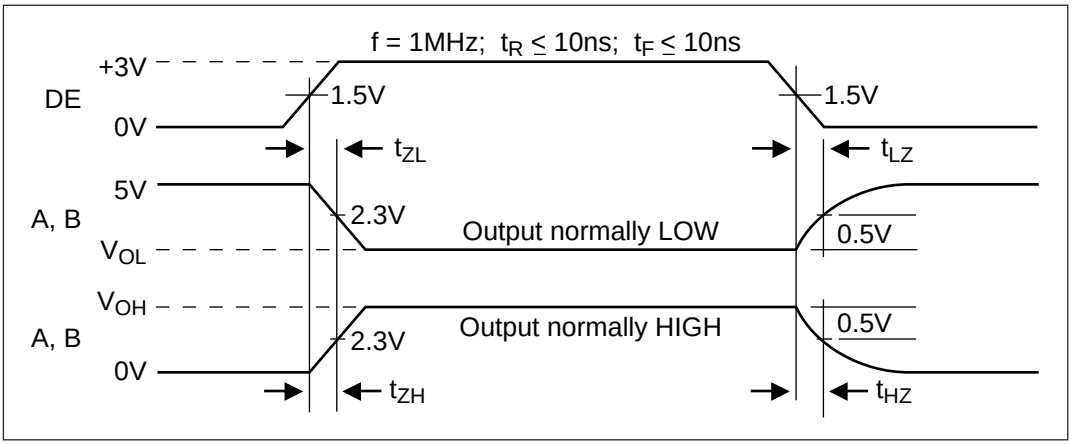



***Figure 6. Driver Enable and Disable Times***

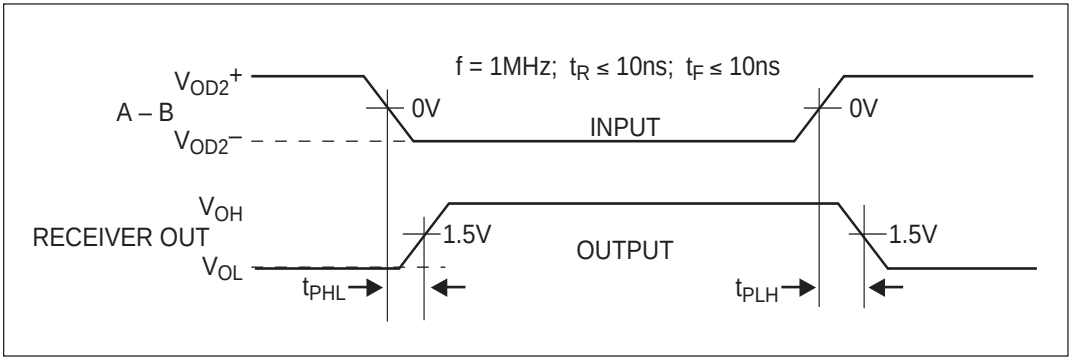



***Figure 7. Receiver Propagation Delays***

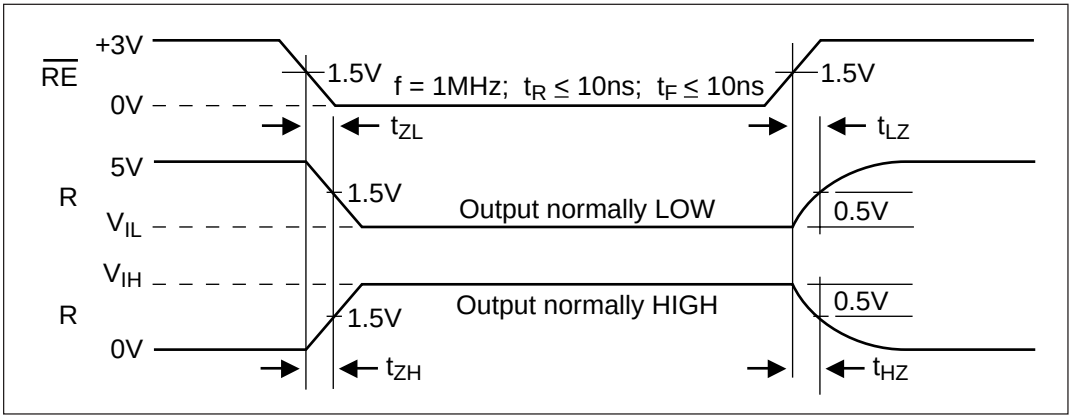
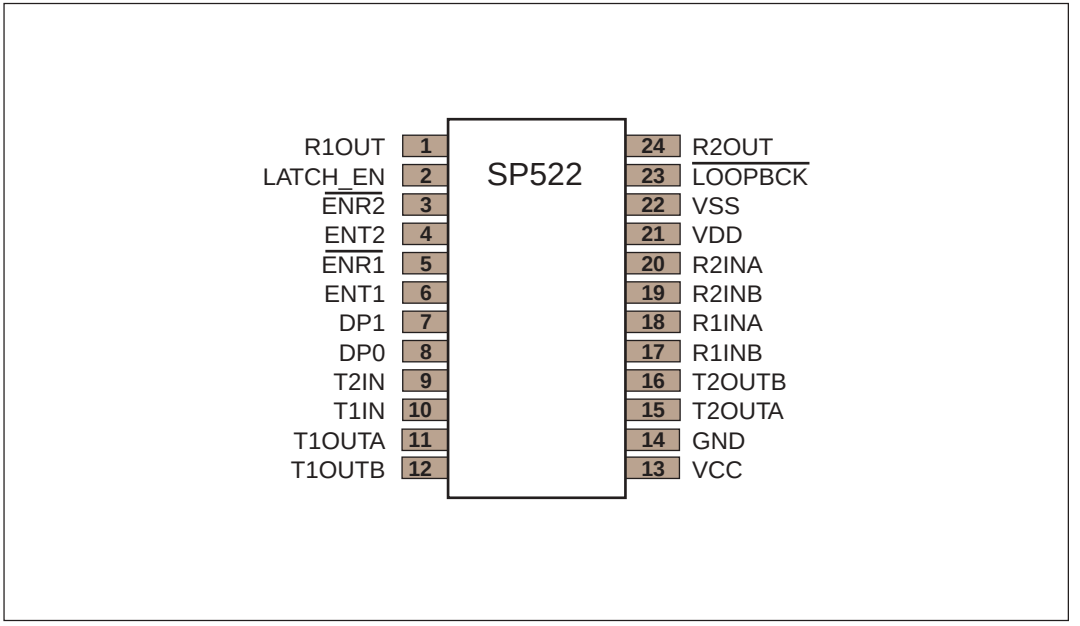


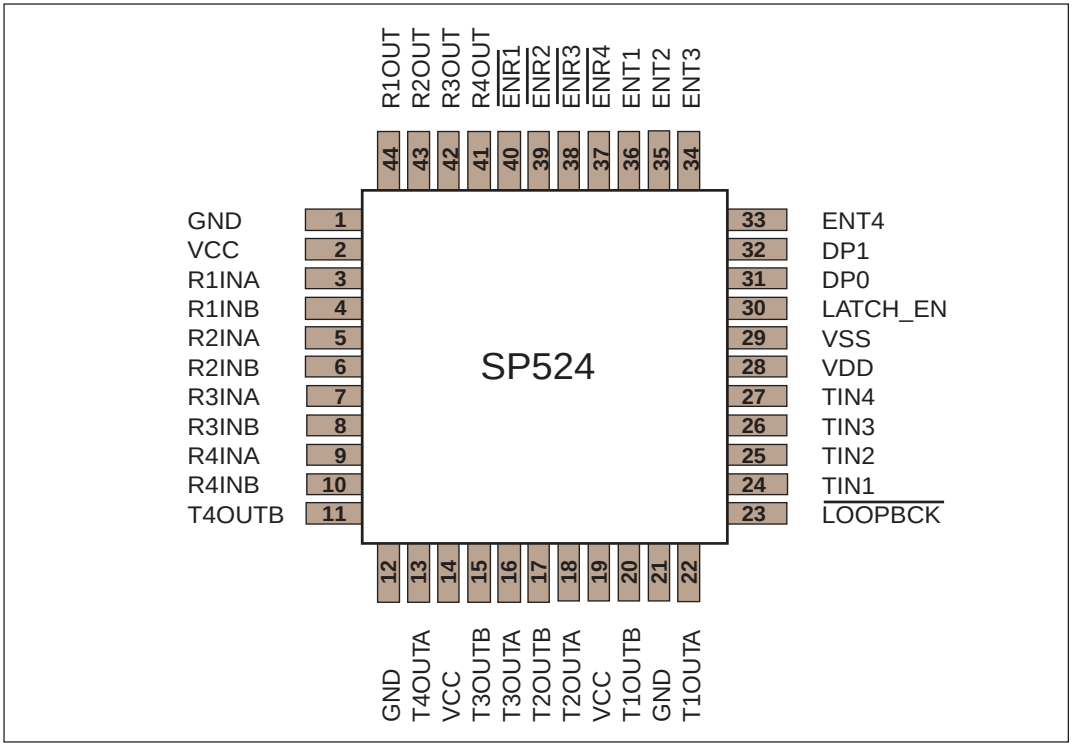

***Figure 8. Receiver Enable and Disable Times***

## PINOUT (24-PIN SOIC & SSOP)




## PINOUT (44-PIN QFP)



## FEATURES

The **SP522** and **SP524** is a highly integrated serial transceiver that offers programmability between interface modes through software control. The **SP522** and **SP524** offers the hardware interface modes for RS-232 (V.28), RS-422A (V.11), RS-423 (V.10), and RS-485. The interface mode selection is done via two control pins. The **SP522** contains two (2) independent drivers and two (2) independent receivers. The **SP524** is basically two **SP522** functions on one silicon, thus having four (4) drivers and four (4) receivers.

The **SP522/SP524** is ideally suited for low-cost wide area network connectivity and other multi-protocol applications. Based on our previous multi-mode SP500 family, **Sipex** has allocated specific transceiver cells or "building blocks" from the SP503 and created the **SP522**. The "building block" concept is that these small transceiver cells can be packaged to offer a simple low-cost solution to networking applications that need only two to four interface modes. The **SP522** can be connected in series to build multiple channels needed for the specific application. **Sipex** has conveniently doubled the **SP522** transceiver cell into the **SP524** on a single silicon. For example in a 8-channel application requiring eight transceivers, the design can be implemented using two **SP524** devices. The **SP522** and **SP524** can also be implemented in series with our SP500 family. An application needing 9-channels can use the SP504 containing seven (7) transceivers with the **SP522**.

## THEORY OF OPERATION

The **SP522** and **SP524** are simply made up of the drivers, receivers, and decoder. The devices operate on three (3) power supplies; $V_{CC}$ at +5V, $V_{DD}$ at +10V , and $V_{SS}$ at –10V. Each of these circuit blocks are described in more detail below.

### Drivers

The **SP522** has two (2) enhanced independent drivers. Control for the mode selection is done via a two–bit control word into DP0 and DP1. The drivers are pre-arranged such that for each mode of operation, the relative position and functionality of the drivers are set up to accommodate the selected interface mode. As the mode of the drivers is changed, the electrical characteristics will change to support the required signal levels. The mode of each driver in the different interface modes that can be selected is shown in *Figures 10 to 13*.

There are three basic types of driver circuits — RS-232, RS-423, and RS-485.

The RS-232 drivers output single–ended signals with a minimum of $\pm$5V (with 3KΩ and 2500pF loading), and can operate up to 120Kbps. The RS-232 drivers are used in RS-232 mode for all signals, and also in V.35 mode where they are used as the control line signals such as DTR and RTS.

The RS-423 drivers are also single–ended signals with a minimum voltage output of $\pm$3.6V (with 450Ω loading) and can operate up to 120Kbps. Open circuit $V_{OL}$ and $V_{OH}$ measurements are $\pm$4.0V to $\pm$6.0V when supplying $\pm$5V to $V_{DD}$ and $V_{SS}$. The RS-423 drivers can be used in RS-449, EIA-530, EIA-530A and V.36 applications as Category II signals from each of their corresponding specifications.

The third type of driver produces a differential signal that can maintain RS-485, $\pm$1.5V differential output levels with a worst case load of 54Ω. The signal levels and drive capability of the RS-485 drivers allow the drivers to also support RS-422 (V.11) requirements of $\pm$2V differential output levels with 100Ω loads. The RS-422 drivers can be used in RS-449, EIA-530, EIA-530A and V.36 applications as Category I signals which are used for clock and data.

The drivers also have separate enable pins which makes the **SP522/SP524** helpful for half-duplex applications. The enable pins will tri-state the drivers when the ENT1 and ENT2 pins are at a logic low ("0"). For the **SP524**, ENT3 and ENT4 are used for the two additional drivers. During tri-stated conditions, the driver outputs will be at a high impedance state.

Unused driver inputs can be left floating; pull–up resistors to +5V is internally connected on the inputs so that the output is at a logic low ("0"). For differential drivers, the non-inverting output will be at a logic high ("1").

## Receivers

The **SP522** has two (2) independent receivers which can be programmed for the different interface modes. Control for the mode selection is done by DP0 and DP1.

Like the drivers, the receivers are pre-arranged for the specific requirements of the interface. As the operating mode of the receivers is changed, the electrical characteristics will change to support the required interface. *Figures 10 to 13* show the mode of each receiver in the different interface modes that can be selected.

There are three basic types of receiver circuits — RS-232, RS-423, and RS-485.

The RS-232 receiver is a single–ended input with a threshold of 0.8V to 3.0V. The RS-232 receiver has an operating voltage range of ±15V and can receive signals up to 120Kbps. The input sensitivity complies with EIA-RS-232 and V.28 at +3V to -3V. The input impedance is 3kΩ to 7kΩ.

The RS-423 receivers are also single–ended but have an input threshold as low as ±300mV. The input impedance is guaranteed to be greater than 4KΩ, with an operating voltage range of ±7V. The RS-423 receivers can operate up to 120Kbps. RS423 receivers can be used in RS-449, EIA530, EIA-530A and V.36 applications as Category II signals as indicated by their corresponding specifications.

The third type of receiver is a differential which supports RS-485. The RS-485 receiver has an input impedance of 15KΩ and a differential threshold of ±300mV. Since the characteristics of an RS-422 (V.11) receiver are actually subsets of RS-485, the receivers for RS-422 requirements are covered by the RS-485 receivers. RS-422 receivers are used in applications for RS-449, EIA530, EIA-530A and V.36 as Category I signals for receiving clock, data, and some control line signals. The differential receivers can receive data up to 10Mbps.

All receivers include a fail-safe feature that output a known logic state when the receiver inputs are unconnected. For single-ended RS-232 receivers, there are internal 5kΩ pull-down resistors on the inputs which produces a logic high ("1") at the receiver outputs. The single-ended RS-423 receivers produce a logic low ("0") on the output when the inputs are open. This is due to a pull-up device connected to the input. The differential receivers have the same internal pull-up device on the non-inverting input which produces a logic high ("1") at the receiver output.

The receivers also have enable pins which allow for convenient half-duplex configurations. The receivers are tri-stated when the $\overline{ENR1}$ and $\overline{ENR2}$ pins are at a logic high ("1"). For the **SP524**, $\overline{ENR3}$ and $\overline{ENR4}$ are used for the additional two receivers.

In addition to the separate enable lines on each transceiver, there is a latch enable pin, LATCH_EN, which is used for enabling and disabling the decoder control inputs (DP0, DP1) and transceiver enable pins. This pin will default to a logic high ("1") if not being used.

## Loopback

The **SP522** and **SP524** contain a loopback feature that allows the driver outputs to "loopback" to the receiver inputs for diagnostic testing in the application. The loopback function is activated when the $\overline{LOOPBCK}$ pin is low. When in loopback mode, the driver outputs are tri-stated and the receiver inputs are deactivated. The receiver input impedance while in loopback will be a minimum of 12kΩ. The loopback function can be initiated during any mode of operation, RS-232, RS-423 or RS-422. The travel path of the transceivers in loopback is shown on *Figure 9*. The loopback function overrides the separate enable pins for the drivers or receivers. When $\overline{LOOPBCK}$ is at a logic low ("0"), the device will be configured in loopback regardless whether the transceiver is enabled or disabled. If the loopback function is not required, the $\overline{LOOPBCK}$ pin will default to a logic high ("1") state.

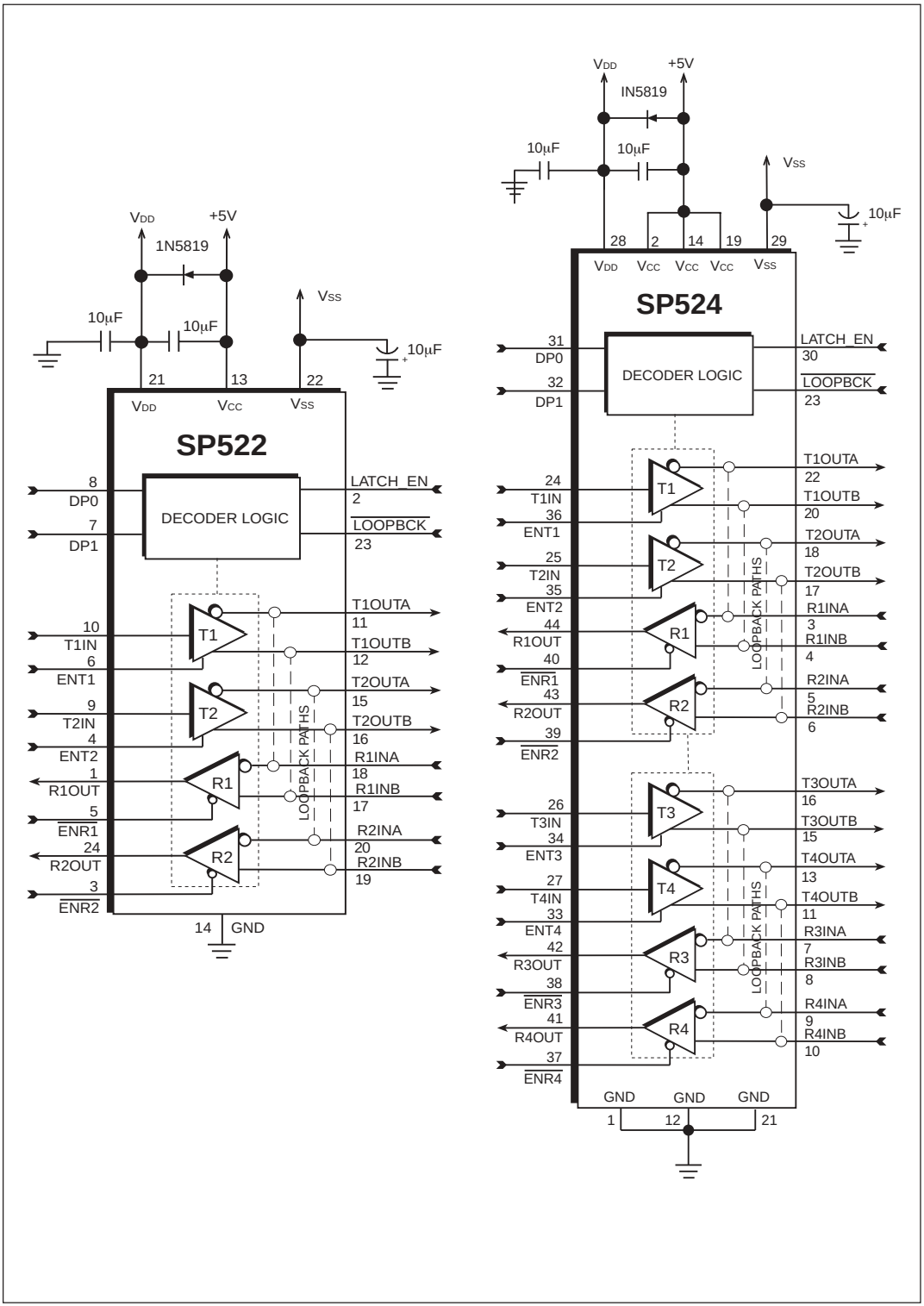
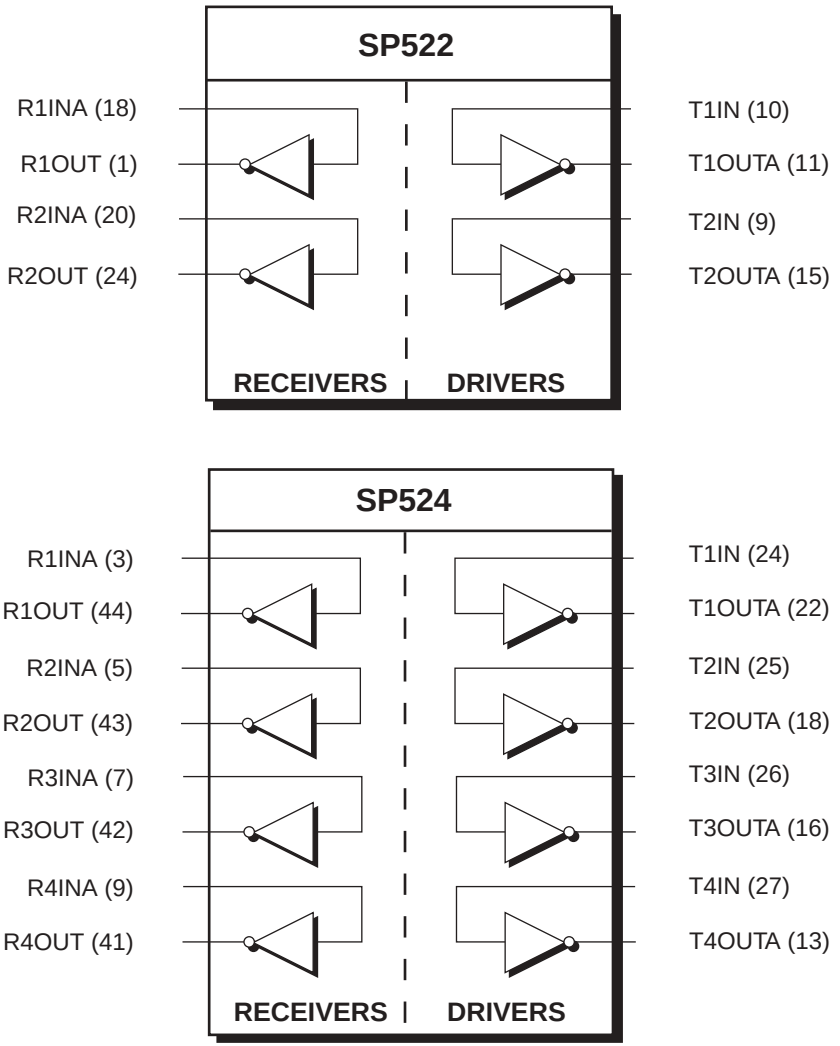



***Figure 9. Typical Operating Circuit, SP522 and SP524***

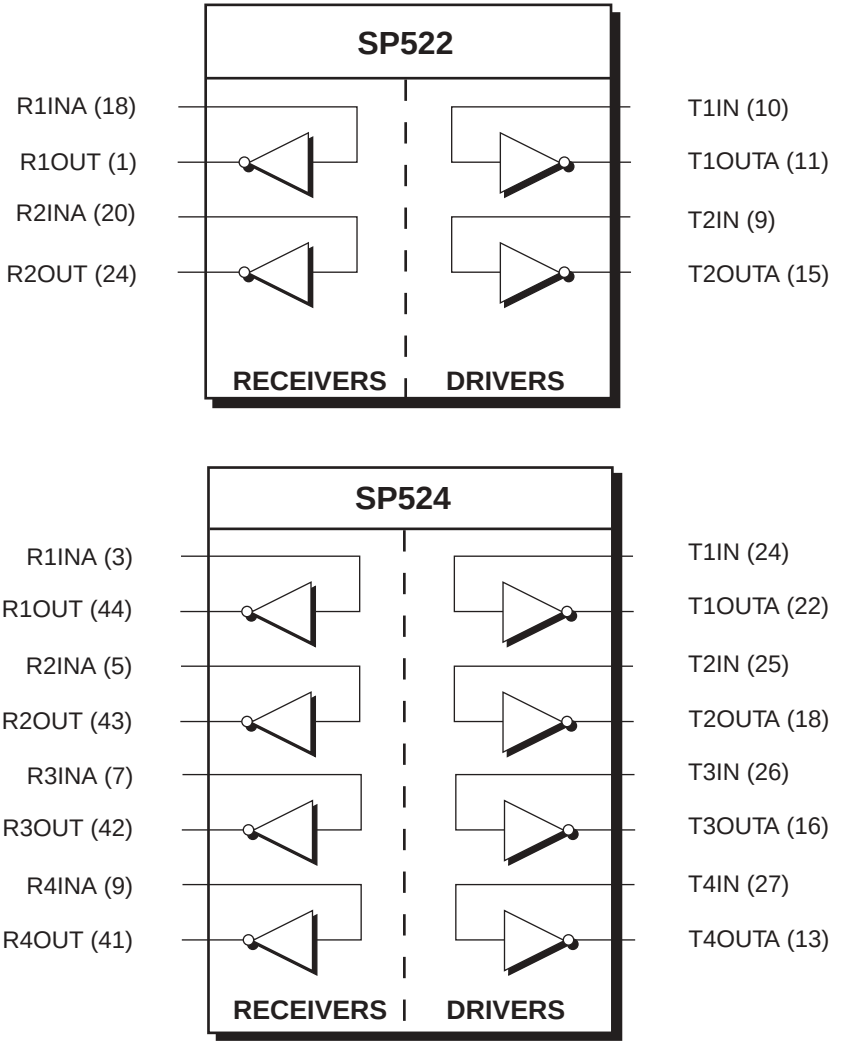
| MODE: RS232 | | | |
|---|---|---|---|
| DRIVER | | RECEIVER | |
| DP0 | DP1 | DP0 | DP1 |
| 1 | 0 | 1 | 0 |




| LATCH_EN | $\overline{\text{LOOPBCK}}$ | ENTx | $\overline{\text{ENRx}}$ |
|---|---|---|---|
| 1 | 1 | 1 | 0 |

***Figure 10. Mode Diagram — RS232***

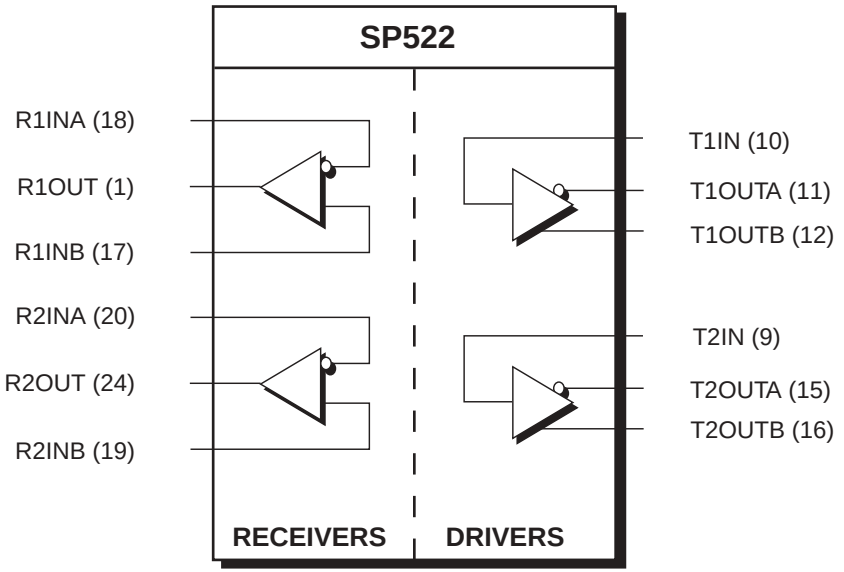
| MODE: RS423 | | | |
|---|---|---|---|
| DRIVER | | RECEIVER | |
| DP0 | DP1 | DP0 | DP1 |
| 1 | 1 | 1 | 1 |




| LATCH_EN | $\overline{\text{LOOPBCK}}$ | ENTx | $\overline{\text{ENRx}}$ |
|---|---|---|---|
| 1 | 1 | 1 | 0 |

***Figure 11. Mode Diagram — RS423***

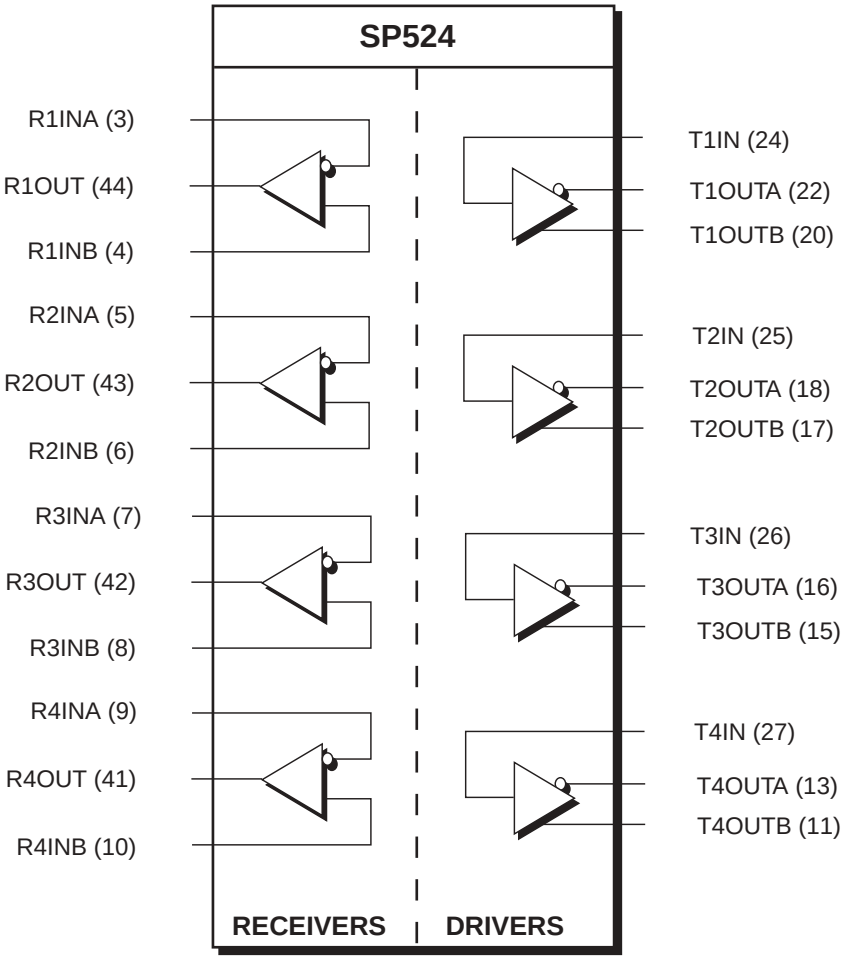
| MODE: RS422/485 | | | |
|---|---|---|---|
| DRIVER | | RECEIVER | |
| DP0 | DP1 | DP0 | DP1 |
| 0 | 1 | 0 | 1 |




| LATCH_EN | $\overline{\text{LOOPBCK}}$ | ENTx | $\overline{\text{ENRx}}$ |
|---|---|---|---|
| 1 | 1 | 1 | 0 |

***Figure 12. Mode Diagram — RS422/RS485 for the SP522***

| MODE: RS422/485 | | | |
|---|---|---|---|
| DRIVER | | RECEIVER | |
| DP0 | DP1 | DP0 | DP1 |
| 0 | 1 | 0 | 1 |




| LATCH_EN | $\overline{\text{LOOPBCK}}$ | ENTx | $\overline{\text{ENR}}$x |
|---|---|---|---|
| 1 | 1 | 1 | 0 |

***Figure 13. Mode Diagram — RS422/RS485 for the SP524***

## APPLICATIONS INFORMATION

### DCE-DTE Applications

A serial port can be easily configured for DTE and DCE using multiple **SP522** and/or **SP524** parts. As shown on *Figure 14*, the transceivers are half-duplexed to provide convenient DCE-DTE capability. The driver outputs are connected to the receiver inputs with only one pair out to the serial port for each driver/receiver. When the driver is tri-stated by applying a logic low ("0") to ENT, the receivers can be active to receive the appropriate input. The driver output during tri-state is high impedance, therefore will not degrade the signal levels of the receiver input signal. When the receiver is tri-stated by applying a logic ("1") to $\overline{ENR}$, the driver output is active to drive the appropriate signal without interference from the receiver. The receiver inputs are at least 12kΩ to ground during tri-state.

### Configuring Additional Multi-Protocol Transceivers

Serial ports usually can have two data signals (SD, RD), three clock signals (TT, ST, RT), and at least eight control signals (CS, RS, etc.). EIA-RS-449 contains twenty six signal types including for a DB-37 connector. A DB-37 serial port design may require thirteen drivers and fourteen receivers. Although many applications do not use all these signals, some applications may need to support extra functions such as diagnostics. Sipex's SP504 supports enough transceivers for the primary channels of data, clock and control signals. Configuring LL, RL and TM may require two additional drivers and one receiver if designing for a DTE (one driver and two receivers for a DCE).

The **SP522** and **SP524** is a convenient solution in a design that requires two extra single ended or differential transceivers. The SP504 and **SP522**, shown in *Figure 15*, can be programmed in various configurations. The SP504 is programmed for RS-449 mode. By connecting the decoder pins of the SP504 to the DP0 and DP1 pins accordingly, the SP522 is programmed in RS-423 mode. This adds two single ended transceivers to the application. For applications needing more than five RS-422 transceivers or more than three RS-423 transceivers, the SP504 can be programmed to RS-422 whereas a SP524 can be added and programmed to RS-423, thus creating seven RS-422 channels and four RS-423 channels. The SP504 and the **SP522/ SP524** can be configured to custom fit the various serial port application needs.

### +5V Only Operation Using the SP782

The **SP522** and **SP524** use external ±10V or ±5V voltage supplies for power to maintain the RS-232 and RS-423 voltage levels, respectively. However, if a low-cost +5V solution if preferred, the **SP522** and **SP524** can be configured with the SP782 or SP784 programmable charge pump. The **Sipex** patent-pending programmable charge pumps offer ±10V or ±5V outputs. The programmability is used for switching from RS-232 using the ±10V outputs to RS-423 using the ±5V outputs. The SP782 requires 0.1µF capacitors and the SP784 requires 10µF capacitors for the charge pump. Please refer to the SP782 and SP784 data sheet for details on the programmable charge pump.

### Achieving ±10V with ±12V Supplies

Since the **SP522** and **SP524** use external ±10V supplies, systems that have ±12V supplies must be regulated down to ±10V. This can be simply configured by placing diodes in series with the $V_{DD}$ and $V_{SS}$ lines. The absolute maximum supply voltage is ±12V. Since most ±12V power supplies have some voltage tolerances, usually ±10%, any increase above the 12V maximum will damage the device. However, the ±12V supply may be used providing that the maximum supply voltages do not exceed the rated absolute maximum $V_{SS}$ and $V_{DD}$.

### Sequencing of Power Supplies

Power Supplies for the **SP522** and **SP524** must be sequenced. The recommended sequence is $V_{CC}$ first, $V_{DD}$ 50-80µSec later and $V_{SS}$ 100 to 1,000µSec after $V_{DD}$. There are no sequencing requirements for the **SP522** or **SP524** when they are powered from either the **SP782** or **SP784** charge pump devices or from the $V_{DD}$ and $V_{SS}$ supply pins of the **SP504** or **SP505** charge pump powered devices. For further details, see the application note, **$V_{DD}$, $V_{CC}$ and $V_{SS}$ Power Supply Sequencing.**

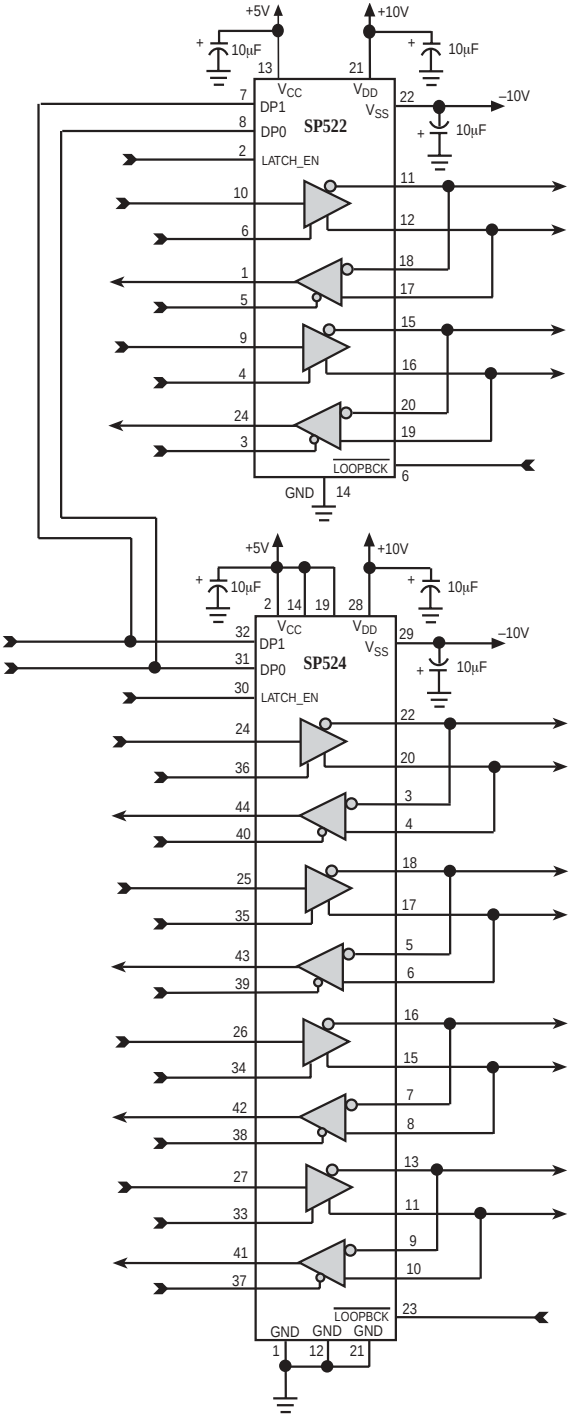
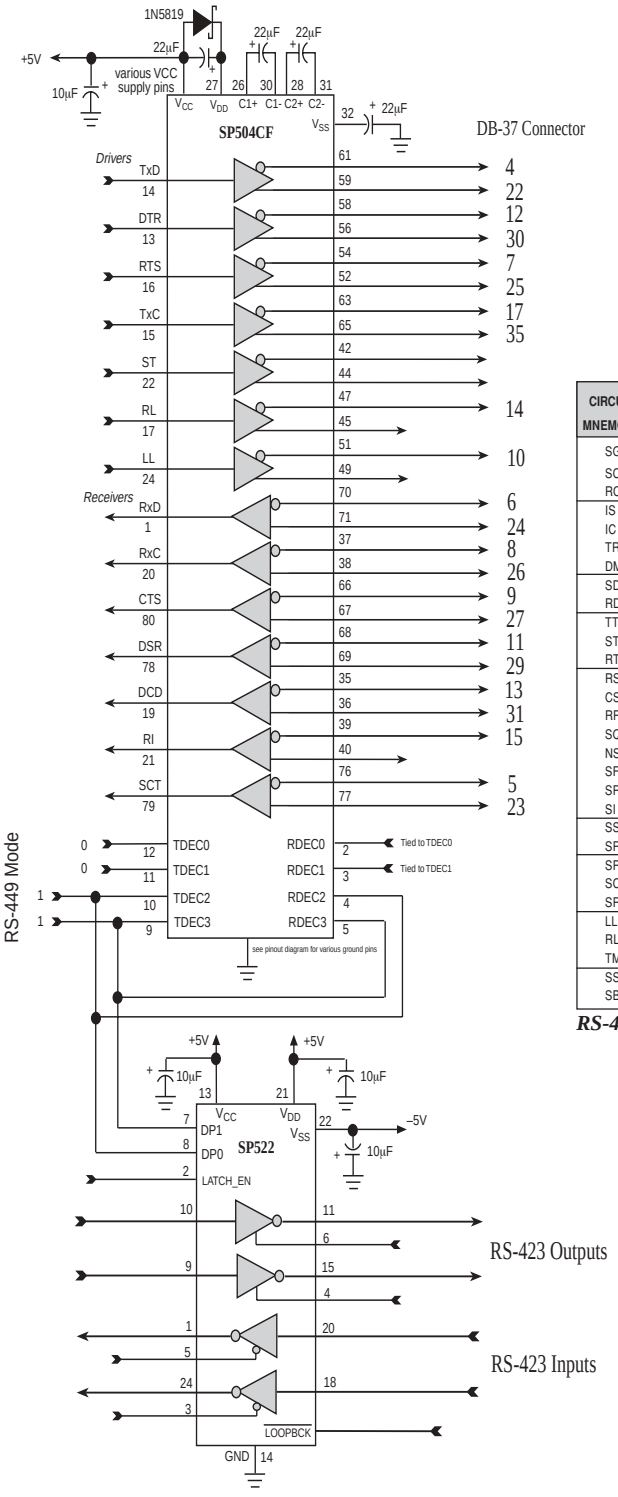



***Figure 14. DTE/DCE Application with the SP522 and SP524***



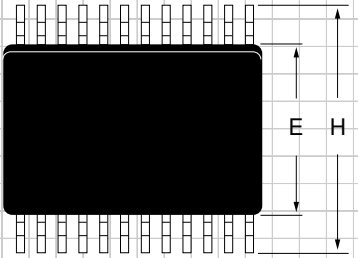

| CIRCUIT MNEMONIC | CIRCUIT NAME | CIRCUIT DIRECTION | CIRCUIT TYPE | |
|---|---|---|---|---|
| SG | SIGNAL GROUND | ---------- | | |
| SC | SEND COMMON | TO DCE | COMMON | |
| RC | RECEIVE COMMON | FROM DCE | | |
| IS | TERMINAL IN SERVICE | TO DCE | | |
| IC | INCOMING CALL | FROM DCE | CONTROL | |
| TR | TERMINAL READY | TO DCE | | |
| DM | DATA MODE | FROM DCE | | |
| SD | SEND DATA | TO DCE | DATA | PRIMARY CHANNEL |
| RD | RECEIVE DATA | FROM DCE | | |
| TT | TERMINAL TIMING | TO DCE | | |
| ST | SEND TIMING | FROM DCE | TIMING | |
| RT | RECEIVE TIMING | FROM DCE | | |
| RS | REQUEST TO SEND | TO DCE | | |
| CS | CLEAR TO SEND | FROM DCE | | |
| RR | RECEIVER READY | FROM DCE | | |
| SQ | SIGNAL QUALITY | FROM DCE | CONTROL | |
| NS | NEW SIGNAL | TO DCE | | |
| SF | SELECT FREQUENCY | TO DCE | | |
| SR | SIGNAL RATE SELECTOR | TO DCE | | |
| SI | SIGNAL RATE INDICATOR | FROM DCE | | |
| SSD | SECONDARY SEND DATA | TO DCE | DATA | SECONDARY CHANNEL |
| SRD | SECONDARY RD | FROM DCE | | |
| SRS | SECONDARY RS | TO DCE | | |
| SCS | SECONDARY CS | FROM DCE | CONTROL | |
| SRR | SECONDARY RR | FROM DCE | | |
| LL | LOCAL LOOPBACK | TO DCE | | |
| RL | REMOTE LOOPBACK | TO DCE | CONTROL | |
| TM | TEST MODE | FROM DCE | | |
| SS | SELECT STANDBY | TO DCE | | |
| SB | STANDBY INDICATOR | FROM DCE | CONTROL | |

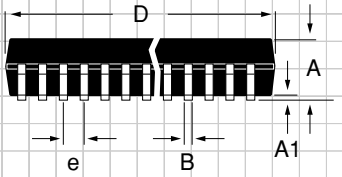
***RS-449 Interchange Circuits Table***

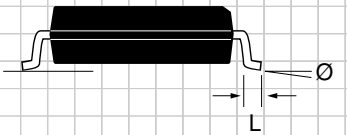
***Figure 15. Adding extra channels using the SP522 and SP504***

## PACKAGE: PLASTIC SMALL OUTLINE (SOIC) (WIDE)

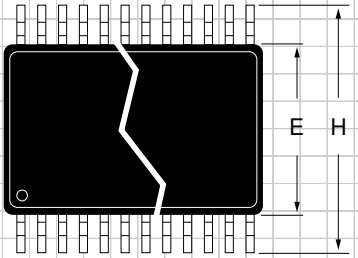


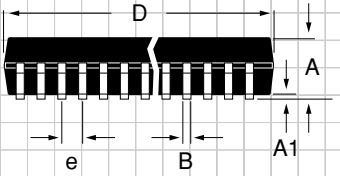




| DIMENSIONS (Inches) Minimum/Maximum (mm) | 24–PIN | | | | | |
|---|---|---|---|---|---|---|
| A | 0.093/0.104 (2.352/2.649) | | | | | |
| A1 | 0.004/0.012 (0.102/0.300) | | | | | |
| B | 0.013/0.020 (0.330/0.508) | | | | | |
| D | 0.599/0.614 (15.20/15.59) | | | | | |
| E | 0.291/0.299 (7.402/7.600) | | | | | |
| e | 0.050 BSC (1.270 BSC) | | | | | |
| H | 0.394/0.419 (10.00/10.64) | | | | | |
| L | 0.016/0.050 (0.406/1.270) | | | | | |
| Ø | 0°/8° (0°/8°) | | | | | |

# PACKAGE: PLASTIC SHRINK SMALL OUTLINE (SSOP)

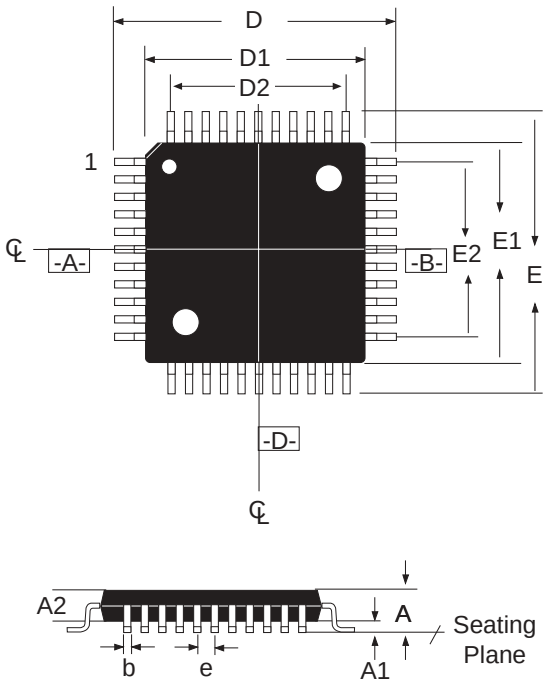


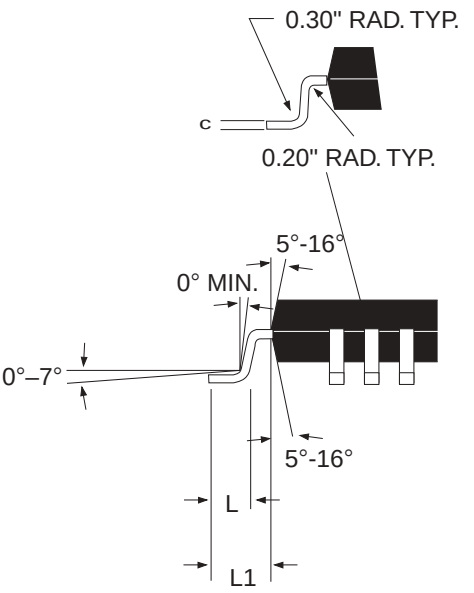





| DIMENSIONS (Inches) Minimum/Maximum (mm) | 24–PIN | | | | | |
|---|---|---|---|---|---|---|
| A | 0.068/0.078 (1.73/1.99) | | | | | |
| A1 | 0.002/0.008 (0.05/0.21) | | | | | |
| B | 0.010/0.015 (0.25/0.38) | | | | | |
| D | 0.317/0.328 (8.07/8.33) | | | | | |
| E | 0.205/0.212 (5.20/5.38) | | | | | |
| e | 0.0256 BSC (0.65 BSC) | | | | | |
| H | 0.301/0.311 (7.65/7.90) | | | | | |
| L | 0.022/0.037 (0.55/0.95) | | | | | |
| Ø | 0°/8° (0°/8°) | | | | | |

## PACKAGE: 44 Pin MQFP



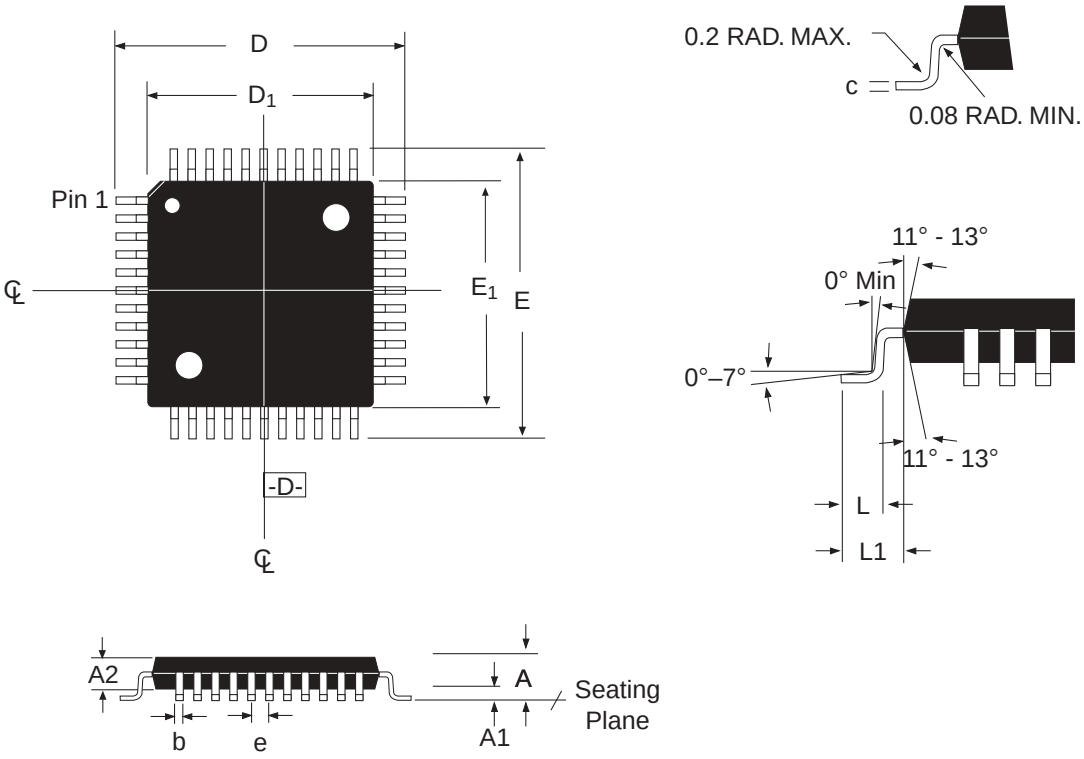




| DIMENSIONS Minimum/Maximum (mm) | 44–PIN MQFP JEDEC MS-022 (AB) Variation | | |
|---|---|---|---|
| SYMBOL | MIN | NOM | MAX |
| A | | | 2.45 |
| A1 | 0.00 | | 0.25 |
| A2 | 1.80 | 2.00 | 2.20 |
| b | 0.29 | | 0.45 |
| D | 13.20 BSC | | |
| D1 | 10.00 BSC | | |
| D2 | 8.00 REF | | |
| E | 13.20 BSC | | |
| E1 | 10.00 BSC | | |
| E2 | 8.00 REF | | |
| e | 0.80 BSC | | |
| N | 44 | | |

| COMMON DIMENTIONS | | | |
|---|---|---|---|
| SYMBL | MIN | NOM | MAX |
| c | 0.11 | | 23.00 |
| L | 0.73 | 0.88 | 1.03 |
| L1 | 1.60 BASIC | | |

**44 PIN MQFP (MS-022 BC)**

## PACKAGE: 44 Pin LQFP




| DIMENSIONS Minimum/Maximum (mm) | 44–PIN LQFP JEDEC MS-026 (BCB) Variation | | |
|---|---|---|---|
| SYMBOL | MIN | NOM | MAX |
| A | | | 1.60 |
| A1 | 0.05 | | 0.15 |
| A2 | 1.35 | 1.40 | 1.45 |
| b | 0.30 | 0.37 | 0.50 |
| D | 12.00 BSC | | |
| D1 | 10.00 BSC | | |
| e | 0.80 BSC | | |
| E | 12.00 BSC | | |
| E1 | 10.00 BSC | | |
| N | 44 | | |

| COMMON DIMENTIONS | | | |
|---|---|---|---|
| SYMBL | MIN | NOM | MAX |
| c | 0.11 | | 23.00 |
| L | 0.45 | 0.60 | 0.75 |
| L1 | 1.00 BASIC | | |

**44 PIN LQFP**

## ORDERING INFORMATION

| Model | Temperature Range | Package Types |
|---|---|---|
| **SP522CT** | 0°C to +70°C | 24-pin SOIC |
| **SP522CA** | 0°C to +70°C | 24-pin SSOP |
| **SP524CF** | 0°C to +70°C | 44-pin MQFP |

Please consult the factory for pricing and availability on a Tape-On-Reel option.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